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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,398	04/14/2004	Jonathan P. Lotz	200314076-1	8467

22879 7590 11/14/2006

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EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,398	LOTZ ET AL.	
	Examiner	Art Unit	
	Dylan White	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-27,29 and 30* is/are rejected.

7)☒ Claim(s) *20 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-19, 21-27, 29-30, are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28, of U.S. Patent No. 7,054,203. Although the conflicting claims are not identical, they are not patentably distinct from each other because the conflicting invention is claimed in a patent which is by the same inventive entity.

Claim 1 can be drawn to claim 1 of US Patent No. 7,054,203 specifically a first settable memory element; a second settable memory element; a voting

structure/settable memory element; where an identical logic value is set in each settable memory element and the voting structure/settable memory element; where the voting structure/settable memory element determines a logical value held on the voting structure/settable memory element after the first settable memory element, the second settable memory element, and the voting structure/settable memory element ate set; where inputs to the voting structure/settable memory element are provided by the first settable memory element, the second settable memory element, and control signals used to set the settable memory element and the voting structure/settable memory element; where a propagation delay through the voting structure/settable memory element is the only propagation delay of the triple redundant latch.

Claim 2 can be drawn to claim 2 of US Patent No. 7,054,203 specifically where the first settable memory elements comprises a transfer gate and a latch.

Claim 3 can be drawn to claim 3 of US Patent No. 7,054,203 specifically where the transfer gate consists of a complementary pass gate.

Claim 4 can be drawn to claim 4 of US Patent No. 7,054,203 specifically where the transfer gate consists of an NFET-only pass gate.

Claim 5 can be drawn to claim 5 of US Patent No. 7,054,203 specifically where the transfer gate consists of a PFET-only transfer gate.

Claim 6 can be drawn to claim 6 of US Patent No. 7,054,203 specifically where the second settable memory element comprises a transfer gate and a latch.

Claim 7 can be drawn to claim 7 of US Patent No. 7,054,203 specifically where the transfer gate consists of a complementary pass gate.

Claim 8 can be drawn to claim 8 of US Patent No. 7,054,203 specifically where the transfer gate consists of an NFET-only pass gate.

Claim 9 can be drawn to claim 9 of US Patent No. 7,054,203 specifically where the transfer gate consists of a PFET-only pass gate.

Claim 10 can be drawn to claim 10 of US Patent No. 7,054,203 specifically where the voting structure/settable memory element comprises a transfer gate, and a latch.

Claim 11 can be drawn to claim 11 of US Patent No. 7,054,203 specifically where the transfer gate consists of a complementary pass gate.

Claim 12 can be drawn to claim 12 of US Patent No. 7,054,203 specifically where the transfer gate consists of an NFET-only pass gate.

Claim 13 can be drawn to claim 13 of US Patent No. 7,054,203 specifically where the transfer gate consists of an PFET-only pass gate.

Claim 14 can be drawn to claim 14 of US Patent No. 7,054,203 specifically a first transfer gate, the first transfer gate having an input, a first control in put, a second control input, and an output; a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output; a third transfer gate, the third transfer gate having an input, a first control input, a second control input, and an output; a first latch, the first latch having an input and an output; a second latch, the second latch having an input and an output; a majority voter/latch, the majority/ latch having an input/output, a first input, a second input, a third input, and a fourth input; where the input of the triple redundant latch is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate; where the output of the triple redundant latch is connected to the input/output of the majority voter/latch; where a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, the first control input of the third transfer gate, and a third input to the majority voter/latch; where a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, and the second control input of the third transfer gate, and the fourth input of the majority voter; where the output of the first transfer gate is connected to the input of the first latch; where the output of the second transfer gate is

connected to the input/output of the majority voter/latch; where the output of the third transfer gate is connected to the input of the second latch; where the output of the first latch is connected to the first input of the majority voter/latch; where the output of the second latch is connected to the second input of the majority voter/latch.

Claim 15 can be drawn to claim 15 of US Patent No. 7,054,203 specifically where the first transfer gate comprises a PFET, the PFET having a gate, a drain, and a source; a NFET, the NFET having a gate, a drain, and a source; where the drains of the PFET and NFET are connected to the input of the first transfer gate; where the sources of the PFET and NFET are connected to the output of the first transfer gate; where the gate of the NFET is connected to the first control input of the first transfer gate; where the gate of the PFET is connected to the second control input of the first transfer gate.

Claim 16 can be drawn to claim 16 of US Patent No. 7,054,203 specifically a PFET, the PFET having a gate, a drain and a source; a NFET, the NFET having a gate, a drain, and a source; where the drains of the PFET and the NFET are connected to the input of the second transfer gate; where the sources of the PFET and the NFET are connected to the output of the second transfer gate; where the gate of the NFET is connected to the first control input of the second transfer gate; where the gate of the PFET is connected to the second control input of the second transfer gate.

Claim 17 can be drawn to claim 17 of US Patent No. 7,054,203 specifically a PFET, the PFET having a gate, a drain and a source; a NFET, the NFET having a gate, a drain and a source; where the drain of the PFET and the NFET are connected to the input of the third transfer gate; where the sources of the PFET and the NFET are connected to the output of the third transfer gate; where the gate of the NFET is connected to the first control input of the third transfer gate; where the get of the PFET is connected to the second control input of the third transfer gate.

Claim 18 can be drawn to claim 18 of US Patent No. 7,054,203 specifically a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a first NFET, the first NFET having a get, a drain and a source; a second NFET, the second NFET having a gate, a drain and a source; where the sources of the first and second PFETs are connected to VDD; where the sources of the first and second NFETs are connected to GND; where the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the first latch; where the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the first latch

Claim 19 can be drawn to claim 19 of US Patent No. 7,054,203 specifically a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a first NFET, the first NFET having a get, a

drain and a source; a second NFET, the second NFET having a gate, a drain and a source; where the sources of the first and second PFETs are connected to VDD; where the sources of the first and second NFETs are connected to GND; where the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the second latch; where the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the second latch.

Claim 21 can be drawn to claim 20 of US Patent No. 7,054,203 specifically where a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a third PFET, the third PFET having a gate, a drain and a source; a first NFET, the first NFET having a gate, a drain and a source; a second NFET, the second NFET having a gate, a drain and a source; a third NFET, the third NFET having a gate, a drain and a source; where the source of the first PFET is connected to VDD; where the source of the third NFET is connected to GND; where the drains of the third PFET and the first NFET are connected to the output of the majority voter; where the gates of the second PFET and the second NFET are connected to the first input of the majority voter; where the gates of the first PFET and the third NFET are connected to the second input of the majority voter; where the gate of the third PFET is connected to the third input of the majority voter; where the gate of the first NFET is connected to the fourth input of the majority voter; where the drain of tie first PFET and the source of the second PFET are connected; where the drain of the

second PFET and the source of the third PFET are connected; where the source of the first NFET and the drain of the second NFET are connected; where the source of the second NFET a and the drain of the third NFET are connected.

Claim 22 can be drawn to claim 21 of US Patent No. 7,054,203 specifically fabricating a first transfer gate, the first transfer gate having an input, a first control input, a second control input and an output; fabricating a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output; fabricating a third transfer gate, the transfer third gate having an input, a first control input, a second control input, and an output; fabricating a first latch, the first latch having an input and an output; fabricating a second latch, the second latch having an input and an output; fabricating a majority voter/latch, the majority/latch having an input/output, a first input, a second input, a third input, and a fourth input; wherein the input of triple redundant latch is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate; wherein a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, the first control input of the third transfer gate, and the third input to the majority voter/latch; wherein a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, the second control input of the third transfer gate, and the fourth input to the majority voter/latch; wherein the output of the first transfer gate is connected to the input of the first latch;

wherein the output of the second transfer gate is connected to the input/output of the majority voter/latch; wherein the output of the third transfer gate is connected to the input of the second latch; wherein the output of the first latch is connected to the first input of the majority voter/latch; wherein the output of the second latch is connected to the second input of the majority voter/latch.

Claim 23 can be drawn to claim 22 of US Patent No. 7,054,203 specifically where the first transfer gate comprises: a PFET, the PFET having a gate, a drain and a source; a NFET, the NFET having a gate, a drain and a source; wherein the drains of the PFET and the NFET are connected to the input of the first transfer gate; wherein the sources of the PFET and the NFET are connected to the output of the first transfer gate; wherein the gate of the NFET is connected to the first control input of the first transfer gate; wherein the gate of the PFET is connected to the second control input of the first transfer gate.

Claim 24 can be drawn to claim 23 of US Patent No. 7,054,203 specifically where the second transfer gate comprises: a PFET, the PFET having a gate, a drain and a source; a NFET, the NFET having a gate, a drain and a source; wherein the drains of the PFET and the NFET are connected to the input of the second transfer gate; wherein the sources of the PFET and the NFET are connected to the output of the second transfer gate; wherein the gate of the NFET is connected to the first control input of the

second transfer gate; wherein the gate of the PFET is connected to the second control input of the second transfer gate.

Claim 25 can be drawn to claim 24 of US Patent No. 7,054,203 specifically where the third transfer gate comprises: a PFET, the PFET having a gate, a drain and a source; a NFET, the NFET having a gate, a drain and a source; wherein the drains of the PFET and the NFET are connected to the input of the third transfer gate; wherein the sources of the PFET and the NFET are connected to the output of the third transfer gate; wherein the gate of the NFET is connected to the first control input of the third transfer gate; wherein the gate of the PFET is connected to the second control input of the third transfer gate.

Claim 26 can be drawn to claim 25 of US Patent No. 7,054,203 specifically where the first latch comprises: a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a first NFET, the first NFET having a gate, a drain and a source; a second NFET, the second NFET having a gate, a drain and a source; wherein the sources of the first and second PFETs are connected to VDD; wherein the sources of the first and second NFETs are connected to GND; wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the first latch; wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the first latch.

Claim 27 can be drawn to claim 26 of US Patent No. 7,054,203 specifically where the second latch comprises: a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a first NFET, the first NFET having a gate, a drain and a source; a second NFET, the second NFET having a gate, a drain and a source; wherein the sources of the first and second PFETs are connected to VDD; wherein the sources of the first and second NFETs are connected to GND; wherein the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input of the second latch; wherein the drain of the first NFET, the drain of the first PFET, the gate of the second NFET, and the gate of the second PFET are the output of the second latch.

Claim 29 can be drawn to claim 27 of US Patent No. 7,054,203 specifically where a first PFET, the first PFET having a gate, a drain and a source; a second PFET, the second PFET having a gate, a drain and a source; a third PFET, the third PFET having a gate, a drain and a source; a first NFET, the first NFET having a gate, a drain and a source; a second NFET, the second NFET having a gate, a drain and a source; a third NFET, the third NFET having a gate, a drain and a source; where the source of the first PFET is connected to VDD; where the source of the third NFET is connected to GND; where the drains of the third PFET and the first NFET are connected to the output of the majority voter; where the gates of the second PFET and the second NFET are connected to the first input of the majority voter; where the gates of the first PFET and

the third NFET are connected to the second input of the majority voter; where the gate of the third PFET is connected to the third input of the majority voter; where the gate of the first NFET is connected to the fourth input of the majority voter; where the drain of tie first PFET and the source of the second PFET are connected; where the drain of the second PFET and the source of the third PFET are connected; where the source of the first NFET and the drain of the second NFET are connected; where the source of the second NFET a and the drain of the third NFET are connected.

Claim 30 can be drawn to claim 2 of US Patent No. 7,054,203 specifically a first means for setting and retaining a logical value; a second means for setting and retaining a logical value; a third means for setting and retaining a logical value; a means for setting a logical value into the third means for setting and retaining a logical value determined by inputs provided by the first and second means for setting and retaining a logical value, and control used to set the means for setting and retaining a logical value; wherein an identical logic value is set in each means for setting and retaining a logical value; wherein a propagation delay through the third means for setting and retaining a logical value is the only propagation delay of the triple redundant latch.

Allowable Subject Matter

Claims 20 and 28 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 20, where the gate of the first NFET, the gate of the second PFET are the input/output of the third latch.

Regarding claim 28, where the gate of the first NFET, the gate of the first PFET, the drain of the second NFET, and the drain of the second PFET are the input/output of the third latch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dylan White
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11/09/06